Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS**

1. **TEMP**
2. **GND**
3. **TRIM**
4. **Vout (Sense)**
5. **Vout (Force)**
6. **Vin**

**.040”**

**6**

**5**

**1**

**2**

**3**

**4**

**ADI**

**1458Y**

**MASK**

**REF**

**.032”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: GND**

**Mask Ref: 1458Y**

**APPROVED BY: DK DIE SIZE .040” X .030” DATE: 6/16/22**

**MFG: ANALOG DEVICES THICKNESS .021” P/N: ADR02NBC**

**DG 10.1.2**

#### Rev B, 7/19/02